REMARKS

Applicant will address each of the Examiner's rejections in the order in which they appear in the Office Action.

Claims Rejections – 35 USC §102

The Examiner rejects Claims 1-2 and 23-27 under 35 USC §102(e) as being anticipated by Cairns. This rejection is respectfully traversed.

In order to advance the prosecution of this application, Applicant has amended Claims 1, 2 and 23-26 to recite "wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate." This is shown, for example, at page 18, lns. 1-5 of the present application.

Applicant does not believe that <u>Cairns</u> discloses or suggests the claimed invention with such a limitation. Accordingly, it is respectfully submitted that the claims are patentable over this reference. Therefore, it is requested that this rejection be withdrawn.

Claim Rejections – 35 USC §103

The Examiner also rejects dependent Claims 3-10 under 35 USC §103 as being unpatentable over Cairns in view of Akebi. The Examiner further rejects dependent Claims 11-22 under 35 USC §103 as being unpatentable over Cairns in view of Yamazaki. These rejections are also traversed.

For at least the reasons described above for the independent claims, these dependent claims are allowable over the cited references. Accordingly, it is respectfully requested that these rejections be withdrawn.

¹ Claim 27 has been canceled rendering the rejection of that claim moot.

$\underline{\mathbb{DS}}$

Applicant is submitting herewith an IDS. It is respectfully requested that this IDS be entered and considered prior to the issuance of a further action in this case.

Amendment B

On December 6, 2002, Applicant submitted Voluntary Amendment B. This amendment was received by the PTO on December 16, 2002, prior to the issuance of the pending Office Action.

Amendment B merely corrected a typographical error in the specification. No new matter was being added by this amendment.

As Applicant does not see any indication of the entrance of this amendment, it is respectfully requested that this amendment now be entered and allowed.

Conclusion

Applicant respectfully submits that the present application is in a condition for allowance and should be allowed.

If any further fee is due for this amendment, please charge our deposit account 50/1039.

Favorable reconsideration is earnestly solicited.

Respectfully submitted,

Mark J. Muzphy

Registration No. 34,225

COOK, ALEX, McFARRON, MANZO, CUMMINGS & MEHLER, Ltd. 200 West Adams Street, Suite 2850 Chicago, Illinois 60606 (312) 236-8500

Marked-up copy of the amendments made herein:

IN THE CLAIMS:

Please amend the claims as follows:

1. (Twice Amended) A display device comprising:

a pixel portion in which (m x 2n) pixels[, each including at least one TFT,] are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, \cdots , Sn, Sn+1, Sn+2, \cdots , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, \cdots , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, $G2R, \cdots, GmR$, wherein:

the pixels connected to the source signal lines S1, S2, \cdots , Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, \cdots , GmL;

the pixels connected to the source signal lines Sn+1, SN+2, \cdots , S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, \cdots , GmR;

the selection signal starts to be supplied to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

the selection signal starts to be supplied to the first gate signal line G2L while the selection signal is supplied to the second gate signal line G1R,

wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate.

2. (Amended) A display device comprising:

a pixel portion in which (m x 2n) pixels[, each including at least one TFT,] are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2,, Sn, Sn+1, Sn+2,, S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L,, GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R,, GmR, wherein:

the pixels connected to the source signal lines S1, S2,, Sn are supplied with the selection signals from the first gate signal lines G1L, G2L,, GmL;

the pixels connected to the source signal lines Sn+1, Sn+2,, S2n are supplied with the selection signals from the second gate signal lines G1R, G2R,, GmR; and

the selection signals are sequentially supplied to the first gate signal line G1L, the second gate signal line G1R, the first gate signal line G2L, the second gate signal line G2R,, the first gate signal line GmL, and the second gate signal line GmR in this order with a delay of a half period between the respective adjacent gate signal lines,

wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate.

23. (Amended) A method of driving an active matrix display device comprising:

a pixel portion in which (m x 2n) pixels[, each including at least one TFT,] are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2,, Sn, Sn+1, Sn+2,, S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L,, GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R,, GmR, wherein said method comprises the steps of:

supplying the pixels connected to the source signal lines S1, S2,, Sn with the selection signals from the first gate signal lines G1L, G2L,, GmL;

supplying the pixels connected to the source signal lines Sn+1, Sn+2,, S2n with the selection signals from the second gate signal lines G1R, G2R,, GmR;

starting to supply the selection signal to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

starting to supply the selection signal to the first gate signal line G1L while the section signal is supplied to the second gate signal line G1R,

wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate.

24. (Twice Amended) A method of driving an active matrix display device comprising:

a pixel portion in which (m x 2n) pixels[, each including at least one TFT,] are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, \cdots , Sn, Sn+1, Sn+2, \cdots , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, ...,

GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, G2R, ..., GmR, wherein said method comprises the steps of:

supplying the pixels connected to the source signal lines S1, S2, \cdots , Sn with the selection signals from the first gate lines G1L, G2L, \cdots , GmL;

supplying the pixels connected to the source signal lines Sn+1, Sn+2, \cdots , S2n with the selection signals from the second gate lines G1R, G2R, \cdots , GmR; and

sequentially supplying the selection signals to the first gate signal line G1L, the second gate signal line G1R, the first gate signal line G2L, the second gate signal line G2R, \cdots , the first gate signal line GmL, and the second gate signal line GmR in this order with a delay of a half period between the respective adjacent gate signal lines,

wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate.

25. (Amended) A display device comprising:

a pixel portion in which (m x 2n) pixels[, each including at least one TFT,] are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, \cdots , Sn, Sn+1, Sn+2, \cdots , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, · · · , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, $G2R, \cdots, GmR$, wherein:

the pixels connected to the source signal lines S1, S2, \cdots , Sn are supplied with the selection signals from the first gate signal lines G1L, G2L, \cdots , GmL;

the pixels connected to the source signal lines Sn+1, SN+2, \cdots , S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, \cdots , GmR;

the selection signal starts to be supplied to the second gate signal line G1R while the selection signal is supplied to the first gate signal line G1L; and

the selection signal starts to be supplied to the first gate signal line G2L while the selection signal is supplied to the second gate signal line G1R,

wherein the m first gate signal lines G1L, G2L, \cdots , GmL of the first gate driver are not connected to the m second gate signal lines G1R, G2R, \cdots , GmR of the second gate driver, and

wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate.

26. (Amended) A display device comprising:

a pixel portion in which (m x 2n) pixels[, each including at least one TFT,] are arranged in matrix form (both m and n are natural numbers);

a source driver for supplying video signals to 2n source signal lines S1, S2, \cdots , Sn, Sn+1, Sn+2, \cdots , S2n;

a first gate driver for supplying selection signals to m first gate signal lines G1L, G2L, \cdots , GmL; and

a second gate driver for supplying selection signals to m second gate signal lines G1R, $G2R, \cdots, GmR$, wherein:

the pixels connected to the source signal lines S1, S2, \cdots , Sn are supplied with the selection

signals from the first gate signal lines G1L, G2L, · · · , GmL;

the pixels connected to the source signal lines Sn+1, SN+2, \cdots , S2n are supplied with the selection signals from the second gate signal lines G1R, G2R, \cdots , GmR;

the selection signal starts to be supplied to one of the i-th gate signal line GiL and the second gate signal line GiR while the selection signal is supplied to the other one of the first gate signal line GiL and the second gate signal line GiR,

wherein each of the pixel portion, the source driver, the first gate driver and the second gate driver comprises at least one TFT formed over a same substrate.

Cancel Claim 27.